What is claimed is:

1. A memory, comprising:

a data bus;

a set of one or more control ports;

a first memory portion comprising a first plurality of storage cells, said first memory portion coupled to said data bus, and capable of being cycled once in an amount of time T;

a second memory portion comprising a second plurality of storage cells, said second memory portion coupled to said data bus, and also capable of being cycled once in said amount of time T; and

an interface coupled to said set of control ports to receive one or more access requests to access either said first memory portion or said second memory portion, each access request comprising a row command and a column command, said interface capable of receiving at least one row command and one column command in an amount of time X, where X is less than or equal to T;

wherein said first memory portion may be accessed at any time relative to accessing of said second memory portion, and vice versa.

2. The memory of claim 1, wherein said first and second memory portions are electrically isolated from each other.

3. The memory of claim 2, wherein said interface is disposed between said first memory portion and said second memory portion to electrically isolate said first memory portion from said second memory portion, and vice versa.

4. The memory of claim 1, wherein said interface is capable of receiving a row command and a column command concurrently.

5. The memory of claim 1, wherein said interface is capable of receiving a row command and a column command in different halves of a clock cycle.

6. The memory of claim 1, wherein said memory is a dynamic memory.

7. The memory of claim 1, wherein said first memory portion further comprises a first set of sense amplifiers, wherein said second memory portion further comprises a second set of sense amplifiers, and wherein said sets of sense amplifiers are electrically isolated from each other such that noise from one set of sense amplifiers does not corrupt data in the other set of sense amplifiers.

8. The memory of claim 7, wherein said first set of sense amplifiers may be activated at any time relative to activation of said second set of sense amplifiers, and vice versa.

9. The memory of claim 7, wherein there is no required minimum time delay between activating said first set of sense amplifiers and activating said second set of sense amplifiers, and vice versa.

10. The memory of claim 7, wherein said first and second sets of sense amplifiers may be activated in consecutive clock cycles.

11. The memory of claim 1, wherein said interface receives a first access request to access said first memory portion, and a second access request to access said second memory portion, wherein said first access request comprises a first row command, and said second access request comprises a second row command, and wherein said interface is capable of receiving said second row command at any time relative to receiving said first row command.

12. The memory of claim 1, wherein said interface receives a first access request to access said first memory portion, and a second access request to access said second memory portion, wherein said first access request comprises a first row command, and said second access request comprises a second row command, and wherein said interface does not require any minimum time delay between receiving said first row command and receiving said second row command.

13. The memory of claim 1, wherein said interface receives a first access request to access said first memory portion, and a second access request to access said

second memory portion, wherein said first access request comprises a first row command, and said second access request comprises a second row command, and wherein said interface may receive said first row command and said second row command in consecutive clock cycles.

14. The memory of claim 1, wherein said one or more access requests comprises a read request.

15. The memory of claim 14, wherein said interface receives and forwards a first access request to said first memory portion, causing said first memory portion to access a first set of data from said first plurality of storage cells, said first set of data having a size no greater than one base granularity, said first memory portion outputting said first set of data onto said data bus, and wherein said interface receives and forwards a second access request to said second memory portion, causing said second memory portion to access a second set of data from said second plurality of storage cells, said second set of data having a size no greater than one base granularity, said second memory portion outputting said second set of data onto said data bus.

16. The memory of claim 15, wherein said second set of data follows said first set of data onto said data bus such that there is substantially no idle time on said data bus between said first set of data and said second set of data.

17. The memory of claim 1, wherein said one or more access requests comprises a write request.

18. The memory of claim 17, wherein said interface receives and forwards a first access request to said first memory portion, causing said first memory portion to obtain a first set of data from said data bus, said first set of data having a size no greater than one base granularity, said first memory portion storing said first set of data into a subset of said first plurality of storage cells, and wherein said interface receives and forwards a second access request to said second memory portion, causing said second memory portion to obtain a second set of data from said data bus, said second set of data having a size no greater than one base granularity, said second memory portion storing said second set of data into a subset of said second plurality of storage cells.

19. The memory of claim 18, wherein said second set of data follows said first set of data on said data bus such that there is substantially no idle time on said data bus between said first set of data and said second set of data.

20. A memory, comprising:

a data bus;

a set of one or more control ports;

a first memory portion comprising a first plurality of storage cells, and a first set of sense amplifiers coupled to said data bus, said first memory portion capable of being cycled once in an amount of time T;

a second memory portion comprising a second plurality of storage cells, and a second set of sense amplifiers coupled to said data bus, said second memory portion also capable of being cycled once in said amount of time T; and

an interface coupled to said set of control ports to receive one or more access requests to access either said first memory portion or said second memory portion, each access request comprising a row command and a column command, said interface capable of receiving at least one row command and one column command in an amount of time X, where X is less than or equal to T;

wherein said first set of sense amplifiers may be activated at any time relative to activation of said second set of sense amplifiers, and vice versa.

21. A method for accessing a memory, comprising:

receiving a first access request on a set of one or more control ports, said first access request comprising a first row command;

in response to said first access request, accessing a first set of storage cells in a first portion of said memory;

receiving a second access request on said set of one or more control ports, said second access request comprising a second row command; and

in response to said second access request, accessing a second set of storage cells in a second portion of said memory;

wherein said second row command may be received at any time relative to receiving said first row command.

22. The method of claim 21, wherein said second row command is received immediately after receiving said first row command.

23. The method of claim 21, wherein said first and second row commands are received in consecutive clock cycles.

24. The method of claim 21, wherein said first and second portions are electrically isolated from each other.

25. The method of claim 21, wherein said first portion comprises a first set of sense amplifiers and said second portion comprises a second set of sense amplifiers, wherein said first set of sense amplifiers is activated in response to said first access request and said second set of sense amplifiers is activated in response to said second access request, and wherein said first set of sense amplifiers may be activated at any time relative to activation of said second set of sense amplifiers, and vice versa.

26. The method of claim 25, wherein said first and second sets of sense amplifiers are electrically isolated from each other such that activation of one set of sense amplifiers does not corrupt data in the other set of sense amplifiers.

27. The method of claim 25, wherein said second set of sense amplifiers is activated immediately after said first set of sense amplifiers.

28. The method of claim 25, wherein said first and second sets of sense amplifiers are activated in consecutive clock cycles.

29. The method of claim 21, wherein said first portion is capable of being cycled once in an amount of time T, and said second portion is capable of being cycled once in said amount of time T, wherein an access request comprises one row command and one column command, and wherein one row command and one column command are received in an amount of time X, where X is less than or equal to T.

30. The method of claim 29, wherein a row command from one access request and a column command from another access request are received in said amount of time X.

31. The method of claim 29, wherein row and column commands are received concurrently.

32. The method of claim 29, wherein row and column commands are received in different halves of clock cycles.

33. The method of claim 21, wherein said first and second access requests are read requests.

34. The method of claim 33, wherein accessing said first set of storage cells in said first portion of said memory comprises:

accessing a first set of data from said first set of storage cells, said first set of data having a size no greater than one base granularity; and

outputting said first set of data onto a data bus.

35. The method of claim 34, wherein accessing said second set of storage cells in said second portion of said memory comprises:

accessing a second set of data from said second set of storage cells, said second set of data having a size no greater than one base granularity; and

outputting said second set of data onto said data bus.

36. The method of claim 35, wherein said second set of data follows said first set of data onto said data bus such that there is substantially no idle time on said data bus between said first set of data and said second set of data.

37. The method of claim 21, wherein said first and second access requests are write requests.

38. The method of claim 37, wherein accessing said first set of storage cells in said first portion of said memory comprises:

obtaining a first set of data from a data bus, said first set of data having a size no greater than one base granularity; and

storing said first set of data into said first set of storage cells.

39. The method of claim 37, wherein accessing said second set of storage cells in said second portion of said memory comprises:

obtaining a second set of data from said data bus, said second set of data having a size no greater than one base granularity; and

storing said second set of data into said second set of storage cells.

40. The method of claim 39, wherein said second set of data follows said first set of data on said data bus such that there is substantially no idle time on said data bus between said first set of data and said second set of data.

41. A method for accessing a memory, comprising:

receiving a first access request on a set of one or more control ports;

in response to said first access request, accessing a first set of data from a first portion of said memory, said first set of data having a size no greater than one base granularity;

sending said first set of data onto a data bus;

receiving a second access request on said set of one or more control ports;

in response to said second access request, accessing a second set of data from a second portion of said memory, said second set of data have a size no greater than one base granularity; and

sending said second set of data onto said data bus following said first set of data such that there is substantially no idle time on said data bus between said first set of data and said second set of data.

42. A method for accessing a memory, comprising:

receiving a first access request on a set of one or more control ports;

in response to said first access request, obtaining a first set of data from a data bus, said first set of data having a size no greater than one base granularity;

storing said first set of data into a first portion of said memory;

receiving a second access request on said set of one or more control ports;

in response to said second access request, obtaining a second set of data from said data bus, said second set of data have a size no greater than one base granularity; and

storing said second set of data into a second portion of said memory;

wherein said second set of data follows said first set of data on said data bus such that there is substantially no idle time on said data bus between said first set of data and said second set of data.

43. In a memory system wherein a memory comprises a first portion and a second portion, a method for controlling access to said memory, comprising:

deriving a first access request to access said first portion of said memory, said first access request comprising a first row command;

deriving a second access request to access said second portion of said memory, said second access request comprising a second row command;

sending said first row command to said memory; and

sending said second row command to said memory;

wherein said second row command may be sent at any time relative to sending said first row command such that no relative timing constraints are imposed between sending said first row command and sending said second row command.

44. The method of claim 43, wherein said second row command is sent immediately after said first row command.

45. The method of claim 43, wherein said first and second row commands are sent in consecutive clock cycles.

46. The method of claim 43, wherein each access request comprises one row command and one column command.

47. The method of claim 46, wherein each of said first and second portions of said memory is capable of being cycled once in an amount of time T, and wherein said second row command and a column command are sent to said memory in an amount of time X, where X is less than or equal to T.

48. The method of claim 47, wherein said second row command and said column command are sent concurrently.

49. The method of claim 47, wherein said second row command and said column command are sent in different halves of a clock cycle.

50. The method of claim 47, wherein said column command is a first column command associated with said first access request.

51. In a memory system wherein a memory comprises a plurality of memory portions, a method for controlling access to said memory, comprising:

deriving a first access request, said first access request being directed to a first memory portion of said memory;

sending said first access request to said memory for processing;

deriving a second access request;

determining whether said second access request is directed to said first memory portion; and

in response to a determination that said second access request is not directed to said first memory portion, sending said second access request to said memory, wherein sending of said second access request need not be constrained by when said first access request was sent.

52. The method of claim 51, wherein said first access request comprises a first row command and said second access request comprises a second row command, and wherein there is no required minimum time delay between sending said first row command and said second row command.

53. The method of claim 52, wherein said second row command is sent immediately after said first row command.

54. The method of claim 52, wherein said first and second row commands are sent in consecutive clock cycles.

55. The method of claim 51, further comprising:

in response to a determination that said second access request is directed to said first memory portion, ensuring that a minimum amount of time has passed since said first access request was sent; and

sending said second access request to said memory after said minimum amount of time has passed.

56. A method for controlling a memory, comprising:

issuing a first row access request to the memory during a first clock cycle of a reference clock;

issuing a column access request to the memory during the first clock cycle; and

issuing a second row access request to the memory during a second clock cycle of the reference clock, wherein the second clock cycle immediately follows the first clock cycle.

57. The method of claim 56, wherein the first row access request and the column access request are issued using a first set of control lines, wherein the first row access request is issued during a first portion of the first clock cycle and the column access request is issued during a second portion of the first clock cycle, wherein the first and second portions are mutually exclusive.

58. The method of claim 56, wherein the first row access request is issued over a first set of control lines and the column access request is issued over a second set of control lines.

59. The method of claim 56, wherein the first row access request corresponds to a portion of a write request, wherein the method further comprises:

sending write data to be written in the memory in response to the write request, wherein the write data is valid for a time period no greater than that of a clock cycle of the reference clock.

60. The method of claim 56, wherein the first row access request corresponds to a portion of a read request, wherein the method further comprises:

receiving read data driven by the memory within a valid data time period that is no greater than that of a clock cycle of the reference clock.

61. The method of claim 56, wherein the first row access request and the column access request correspond to different memory access requests.

62. A memory system, comprising:

a memory, comprising:

a data bus;

a set of one or more control ports;

a first memory portion comprising a first plurality of storage cells, said first memory portion coupled to said data bus, and capable of being cycled once in an amount of time T;

a second memory portion comprising a second plurality of storage cells, said second memory portion coupled to said data bus, and also capable of being cycled once in said amount of time T; and

an interface coupled to said set of control ports to receive one or more access requests to access either said first memory portion or said second memory portion, each access request comprising a row command and a column command, said interface capable of receiving at least one row command and one column command in an amount of time X, where X is less than or equal to T;

wherein said first memory portion may be accessed at any time relative to accessing of said second memory portion, and vice versa; and

a controller coupled to said data bus and said set of one or more control ports to control operation of said memory, said controller capable of sending at least one row command and one column command to said memory in said amount of time X, and capable of sending a first row command to access

said first memory portion and a second row command to access said second memory portion at any time relative to each other such that no relative timing constraints are imposed between sending said first row command and sending said second row command.

63. The memory system of claim 62, wherein said first and second memory portions are electrically isolated from each other.

64. The memory system of claim 63, wherein said interface is disposed between said first memory portion and said second memory portion to electrically isolate said first memory portion from said second memory portion, and vice versa.

65. The memory system of claim 62, wherein said controller sends said second row command immediately after sending said first row command.

66. The memory system of claim 62, wherein said controller sends said first and second row commands in consecutive clock cycles.

67. The memory system of claim 66, wherein said first and second memory portions may be accessed in consecutive clock cycles.

68. The memory system of claim 62, wherein said first memory portion further comprises a first set of sense amplifiers, and said second memory portion further

comprises a second set of sense amplifiers, and wherein said first set of sense amplifiers may be activated at any time relative to activation of said second set of sense amplifiers, and vice versa.

69. The memory system of claim 68, wherein said first and second sets of sense amplifiers are electrically isolated from each other.

70. The memory system of claim 68, wherein there is no required minimum time delay between activating said first set of sense amplifiers and activating said second set of sense amplifiers, and vice versa.

71. The memory system of claim 68, wherein said controller sends said first and second row commands in consecutive clock cycles.

72. The memory system of claim 71, wherein said first set of sense amplifiers and said second set of sense amplifiers may be activated in consecutive clock cycles.